UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LUAN TRAN, D. MARK DURCAN, TYLER A. LOWREY, ROB B. KERR, and KRIS K. BROWN

Appeal No. 2005-2155
Application No. 10/059,727

ON BRIEF

Before HAIRSTON, GROSS, and NAPPI, ***Administrative Patent Judges.***

GROSS, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 8 and 10 through 25.

Appellants' invention relates to a semiconductor memory array. Claim 11 is illustrative of the claimed invention, and it reads as follows:

11. A memory device comprising:

memory cells each having an area of about $6F^2$;

sense amplifiers;

bit lines coupled to the sense amplifiers in a folded bit line arrangement;

active area lines; and

transistors formed in the active area lines and electrically coupling corresponding memory cells to corresponding bit lines.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Chu et al. (Chu)	5,107,459	Apr. 21, 1992
Aoki et al. (Aoki)	5,747,844	May 05, 1998

Claims 1 through 8 and 10 through 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Aoki in view of Chu.

Reference is made to the Examiner's Answer (Paper No. 12, mailed March 9, 2004) for the examiner's complete reasoning in support of the rejection, and to appellants' Brief (Paper No. 10, filed November 20, 2003) and Reply Brief (filed May 10, 2004) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1 through 8 and 10 through 25.

Appellants argue (Brief, page 13) that Aoki teaches that folded bit line arrangements are space inefficient and chooses an

open bit line configuration instead. Appellants continue (Brief, page 14) that Aoki did not recognize that a $6F^2$ memory cell could be achieved with a folded bit line arrangement, nor did Chu suggest such. Therefore, appellants conclude (Brief, page 14) that a prima facie case of obviousness has not been established. We agree.

The examiner (Answer, pages 3-4) relies primarily on Aoki, adding Chu for bit lines including first and second level portions that are vertically separated from one another. The examiner admits (Answer, page 4) that Aoki fails to disclose a dimension of $6F^2$ for a folded bit line configuration. The examiner asserts (Answer, page 4) that such dimensions were known, as disclosed by Keeth, which is not included in the statement of the rejection. The examiner concludes (Answer, page 4) that it would have been obvious to "scale a folded bit line to a smaller size for the purpose, for example, of enhancing the integration density of the MOS device."

The Court in ***In re Hoch***, 428 F.2d 1341, n. 3, 166 USPQ 406, n. 3 (CCPA 1970), held that "[w]here a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including the reference in the statement of rejection." The Court affirmed the

rejection in that case because the references relied upon but not included in the statement of the rejection were not needed to meet the limitations of the claims. Here, however, the examiner relies upon Keeth (Answer, pages 4, 6, and 7) and Mori (Answer, page 7) to show the inventive concept (i.e., in a major capacity), without including them in the statement of the rejection. Thus, in accordance with ***Hoch***, we will not consider Keeth or Mori, as they are not properly before us.

In the Response to Arguments section of the Answer, the examiner states (Answer, page 6), "The size dimension in this application cannot be considered the sole determining factor for patentability." The examiner relies on ***In re Rose***, 220 F.2d 459, 105 USPQ 237 (CCPA 1955), and ***Gardner v. TEC Systems, Inc.***, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), as support for the proposition that a difference in size is not patentable. The examiner explains (Answer, page 7) that the Court in ***Gardner*** held that merely a difference in size with no difference in performance is not patentably distinct from the prior. The examiner asserts in the next paragraph that "[t]here is no argument that the claimed $6F^2$ device will function in a different manner than the $8F^2$ device of Aoki." We disagree with the examiner's assumptions. Appellants argue (Reply Brief, pages 5-

6) that the $6F^2$ device will function differently than the $8F^2$ device. Therefore, the difference in dimension can render the claims patentably distinct over the prior art.

Without Keeth and Mori, we find nothing in either Aoki or Chu, nor any convincing explanation in the Examiner's Answer, that would suggest a folded bit line configuration with a $6F^2$ dimension. Therefore, we cannot sustain the rejection of independent claims 1, 11, 18, and 19, all of which recite memory cells having an area of about $6F^2$ in a folded bit line arrangement, nor of their dependents, claims 2 through 8, 10, 12 through 17, and 20 through 25.

CONCLUSION

The decision of the examiner rejecting claims 1 through 8 and 10 through 25 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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ANITA PELLMAN GROSS) BOARD OF PATENT
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) INTERFERENCES
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